Q.1

a. Explain short channel effect in MOSFET.

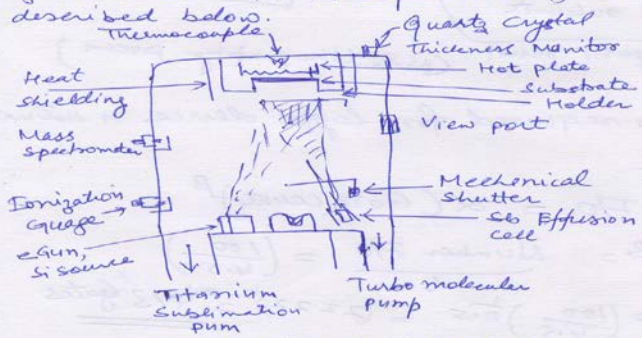
Answer:

1 (a) The short channel effect is the decrease in MOSFET threshold voltage as the channel length is reduced. It is essentially pronounced when the drain is biased at a voltage equal to that of the power supply. In a CMOS VLSI technology, channel length varies statistically from chip to chip, wafer to wafer and lot to lot due to process tolerances. The short channel effect is therefore, an important consideration in device design. The threshold voltage should not become too low for minimum channel-length device on chip. The variation of threshold voltage of n MOSFET and PMOSFET versus channel length is shown below

b. Describe molecular beam epitaxy method to grow crystal.

Answer:

(b) Molecular beam epitaxy (MBE) is a non chemical vapour deposition epitaxial process that uses an evaporation method. The essence of the method is an evaporation of silicon and one or more dopants, as described below.



Schematic of MBE growth system

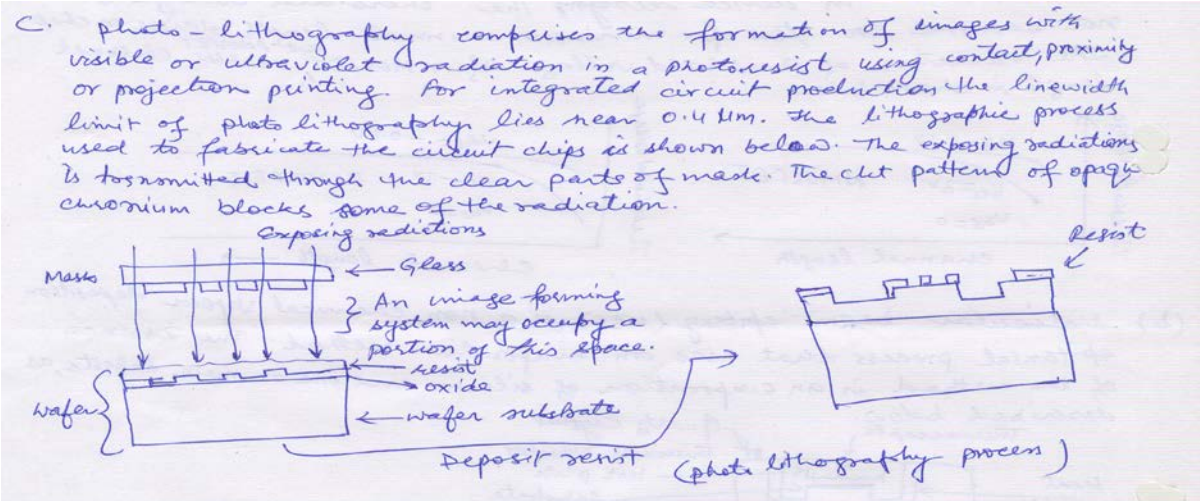
The evaporated species are transported at a relatively high velocity in vacuum to the substrate. The relative low vapour pressure of Si and the dopant ensures consideration at low temperature substrate. The Silicon MBE is performed under ultra high vacuum conditions of 10^{-8} to 10^{-10} torr. The mean free path of atoms is

$L = 5 \times 10^{-3}/p$.

Because of collision between atoms are unimportant in a high vacuum, the transport velocity is controlled by thermal energy effects than by diffusion effects. MBE doping has several features. A wider choice of dopants can be used, more control of doping profile is possible.

c. Explain photo- lithography process to fabricate circuit chips.

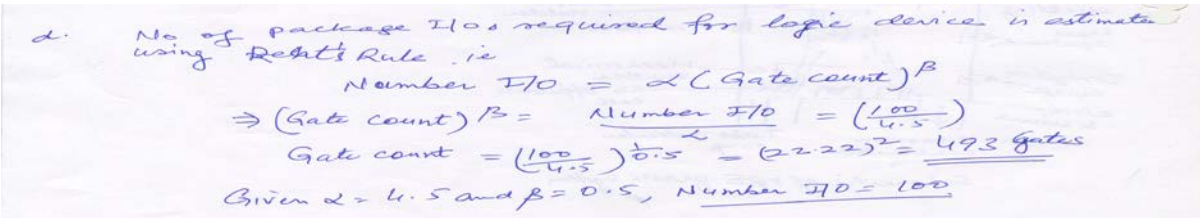
Answer:



c. photo-lithography comprises the formation of images with visible or ultraviolet radiation in a photoresist using contact, proximity or projection printing. For integrated circuit production the linewidth limit of photolithography lies near 0.4 μm. The lithographic process used to fabricate the circuit chips is shown below. The exposing radiations is transmitted through the clear parts of mask. The dot pattern of opaque chromium blocks some of the radiation.

d. Estimate the number of gates that can be included on a logic – gate array chip which is to be assembled in a 100 I/O package. Assume $\alpha = 4.5$ and $\beta = 0.5$

Answer:



d. No of package I/Os required for logic device is estimated using Rent's Rule. ie

$$\text{Number I/O} = \alpha(\text{Gate count})^{\beta}$$

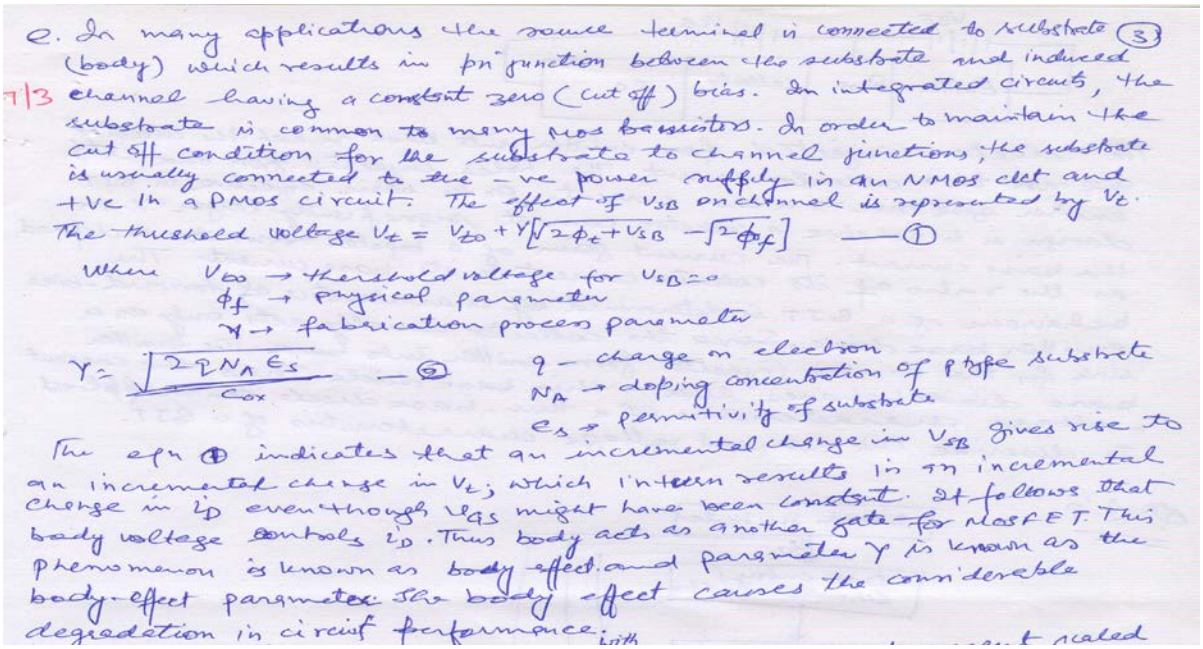
$$\Rightarrow (\text{Gate count})^{\beta} = \frac{\text{Number I/O}}{\alpha} = \left(\frac{100}{4.5}\right)$$

$$\text{Gate count} = \left(\frac{100}{4.5}\right)^{\frac{1}{0.5}} = (22.22)^2 = 493 \text{ Gates}$$

Given $\alpha = 4.5$ and $\beta = 0.5$, Number I/O = 100

e. Explain body effect in MOSFET.

Answer:



e. In many applications the source terminal is connected to substrate (body) which results in pn junction between the substrate and induced channel having a constant zero (cut off) bias. In integrated circuits, the substrate is common to many MOS transistors. In order to maintain the cut off condition for the substrate to channel junctions, the substrate is usually connected to the –ve power supply in an NMOS ckt and +Ve in a PMOS circuit. The effect of V_{SB} on channel is represented by V_t.

The threshold voltage $V_t = V_{to} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$ —①

Where V_{to} → threshold voltage for $V_{SB} = 0$

ϕ_f → physical parameter

γ → fabrication process parameter

$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \quad —②$$

q – charge on electron

N_A → doping concentration of p type substrate

ϵ_s → permittivity of substrate

The eqn ① indicates that an incremental change in V_{SB} gives rise to an incremental change in V_t, which in turn results in an incremental change in i_D even though V_{GS} might have been constant. It follows that body voltage controls i_D. Thus body acts as another gate for MOSFET. This phenomenon is known as body effect and parameter γ is known as the body-effect parameter. The body effect causes the considerable degradation in circuit performance with scaled

f. Explain the effect of scaling on circuit parameters.
Answer:

degradation in circuit performance.

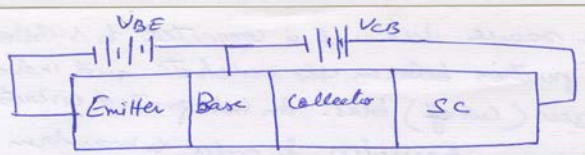
f. Effect of scaling on circuit parameters:- With Both voltage and current scaled down by some factor, the active channel resistance of the scaled down device remains unchanged. It is further assumed that parasitic resistance is either negligible in scaling. The circuit delay, which is proportional to RC or CV/I then scales down by k. Thus, Once the device dimensions and power supply voltage are scaled down, the ckt speeds up by some factor Moreover, power dissipation per circuit, which is proportional to VI, is reduced by k^2. Since the circuit density has increased by k^2, the power density remains unchanged in the scaled down device. The power-delay product of scaled cmos circuit shows a dramatic improvement by a factor of k^3.

diodes connected

g. Explain two PN diode model of BJT.
Answer:

improvement by a factor of k^3.

g. PN diode model of BJT: BJT consists of two PN diodes connected back to back. The basic operation of BJT can be described by operation back to back-diodes. To turn PNP transistor on, the emitter base diode is forward biased resulting in holes being injected from base into the emitter and electrons being injected from emitter to base. In normal operation, base-collector diode is reverse biased so that there is no forward current flow in the base-collector diode. The bias condition is shown below.

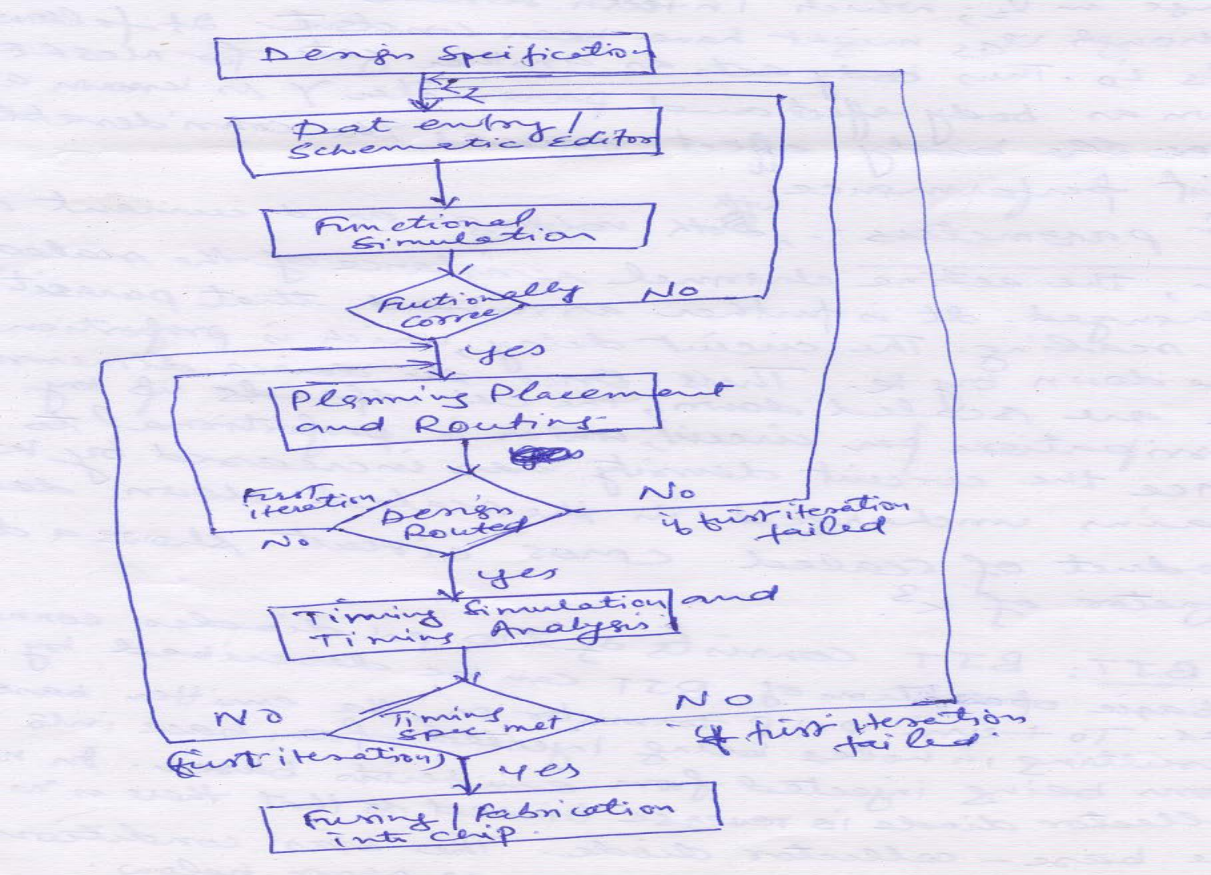


The electrons injected from emitter into base reach the collector give rise to a collector current. The holes injected from base into emitter give rise to a base current. On the basic objective in BJT design is to achieve a collector current significantly larger than the base current. The current gain of a bipolar transistor is defined as the ratio of its collector current to its base current. The behaviour of a BJT is determined by characteristics of forward-bias emitter base diode, Since the collector usually acts only as a sink for the carrier injected from emitter into base. The emitter base diode behaves like a thin base diode. Thus the current voltage characteristics of a thin-base diode can be applied to describe the current voltage characteristics of a BJT.

Q.2

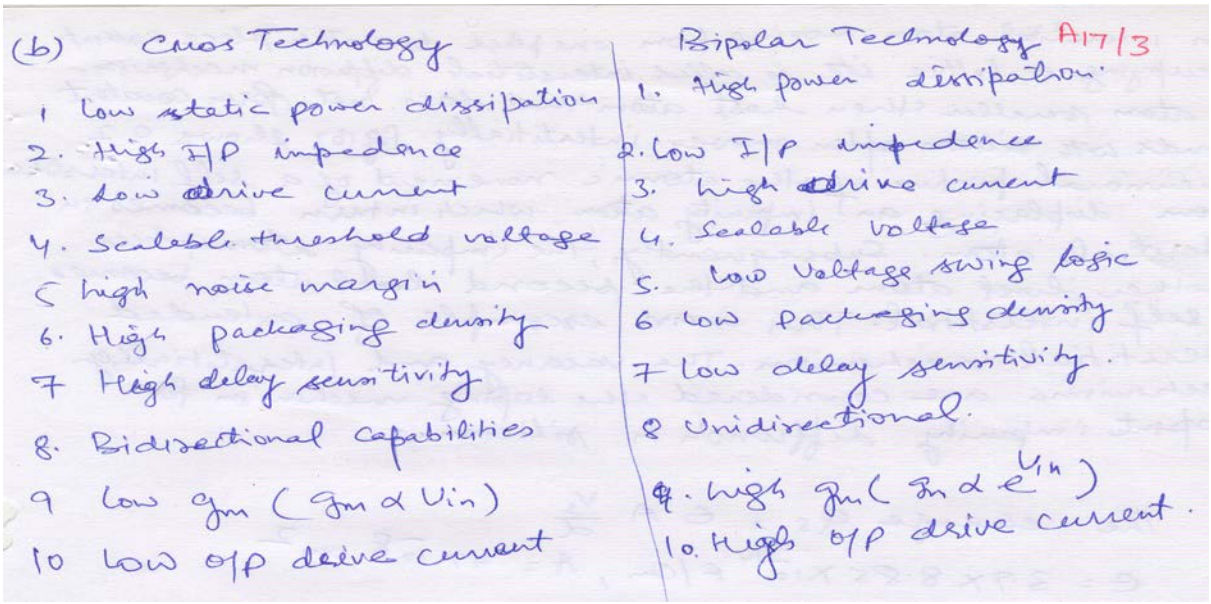
a. Explain VLSI design flow.

Answer:



b. Give the comparison between CMOS and bipolar technologies.

Answer:



(b) CMOS Technology

1. Low static power dissipation
2. High I/P impedence
3. Low drive current
4. Scalable threshold voltage
5. High noise margin
6. High packaging density
7. High delay sensitivity
8. Bidirectional capabilities
9. Low g_m ($g_m \propto V_{in}$)
10. Low o/p drive current

Bipolar Technology A17/3

1. High power dissipation
2. Low I/P impedence
3. High drive current
4. Scalable voltage
5. Low voltage swing logic
6. Low packaging density
7. Low delay sensitivity.
8. Unidirectional.
9. High g_m ($g_m \propto e^{V_{in}}$)
10. High o/p drive current.

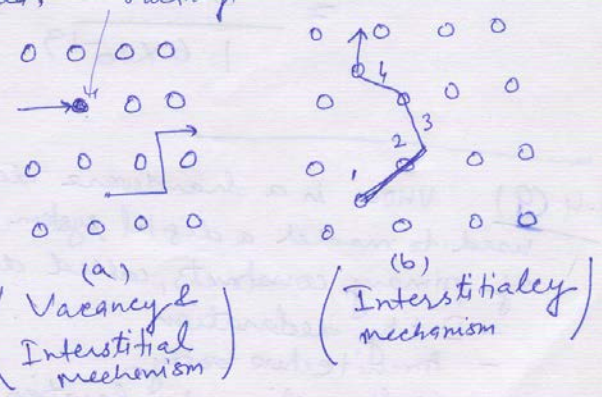
Q.3

a.What is diffusion? Explain models of diffusion in solids.

Answer:

Q.3(a) Diffusion :- Diffusion means to alter the type of conductivity in silicon or germanium. It is process of inducing dopant into silicon by is known as diffusion.

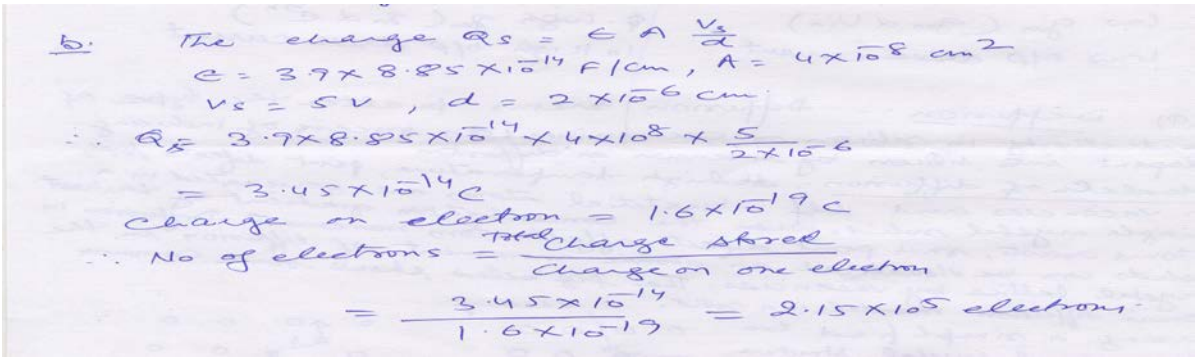
Models of diffusion: At high temperature, point defects such as vacancies and self interstitial atoms are generated in a single crystal solid. When the concentration gradient of the host atoms exists, such point defects affect atom movement. Diffusion in solids can be visualized as atomic movement of diffusion in the crystal lattice by vacancies. The fig below shows some common atomic diffusion models in a solid, using a simplified two dimensional crystal structure with lattice constant a. The open circles represent the host atoms occupying low temperature lattice positions.



An interstitial atom moving from one place to another place without occupying a lattice site is called interstitial diffusion mechanism. An atom smaller than host atom that does not form covalent bonds with silicon often moves interstitially. Fig (b) shows a 2 dimensional picture of the atomic movement of a self interstitial atom displacing an impurity atom which in turn becomes an interstial atom. Subsequently, the impurity atom displaces another host atom and the second host atom becomes a self interstitial. This is an example of extended interstitial mechanism. The vacancy and interstitialcy mechanisms are considered the doping mechanism for dopant impurity diffusion in silicon.

b. What is the stored charge and number of electrons on an MOS capacitor with an area of 4 μm^2 a dielectric of 200 Aº thick S_iO_2 and applied voltage of 5V?

Answer:



b. The charge $Q_S = \epsilon A \frac{V_s}{d}$

$\epsilon = 3.9 \times 8.85 \times 10^{-14}$ F/cm, $A = 4 \times 10^{-8}$ cm^2

$V_s = 5$ V, $d = 2 \times 10^{-6}$ cm

$\therefore Q_s = 3.9 \times 8.85 \times 10^{-14} \times 4 \times 10^{-8} \times \frac{5}{2 \times 10^{-6}}$

$= 3.45 \times 10^{-14}$ C

Charge on electron $= 1.6 \times 10^{-19}$ C

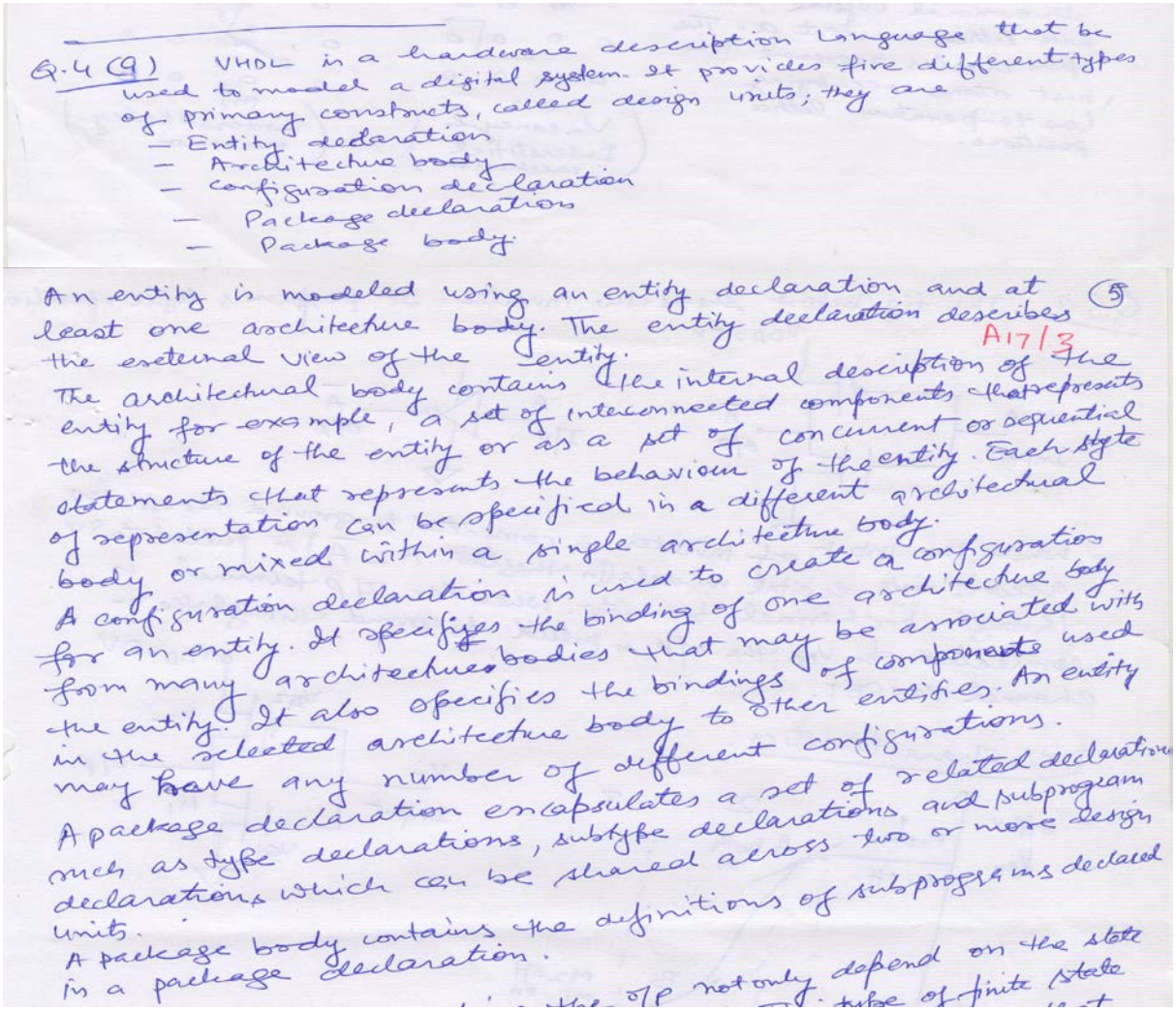
$\therefore$ No of electrons $= \frac{\text{Total charge stored}}{\text{Charge on one electron}}$

$= \frac{3.45 \times 10^{-14}}{1.6 \times 10^{-19}} = 2.15 \times 10^5$ electrons

Q.4

a. How VHDL is used to model the digital.

Answer:



Q.4 (a) VHDL is a hardware description language that be used to model a digital system. It provides five different types of primary constructs, called design units; they are

- Entity declaration
- Architecture body
- configuration declaration
- Package declaration
- Package body

An entity is modeled using an entity declaration and at least one architecture body. The entity declaration describes the external view of the entity. (5)

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The architectural body contains the internal description of the entity for example, a set of interconnected components that represents the structure of the entity or as a set of concurrent or sequential statements that represents the behaviour of the entity. Each style of representation can be specified in a different architectural body or mixed within a single architecture body.

A configuration declaration is used to create a configuration for an entity. It specifies the binding of one architecture body from many architecture bodies that may be associated with the entity. It also specifies the bindings of components used in the selected architecture body to other entities. An entity may have any number of different configurations.

A package declaration encapsulates a set of related declarations such as type declarations, subtype declarations and subprogram declarations which can be shared across two or more design units.

A package body contains the definitions of subprograms declared in a package declaration.

b. Give state transition table for Mealy machine.

Answer:

units.
A package body contains the digital
is a package declaration.

b. In a Mealy finite machine, the o/p not only depend on the state of the machine but also on its inputs. This type of finite state machine can also be modeled in a style similar to that of the Moore machine. The state transition table for Mealy machine

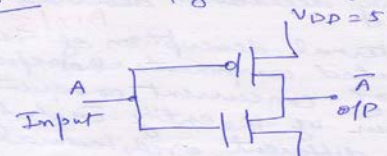
	0	1
ST0	ST0 / 0	ST3 / 1
ST1	ST1 / 1	ST0 / 0
ST2	ST2 / 0	ST1 / 1
ST3	ST2 / 0	ST1 / 0

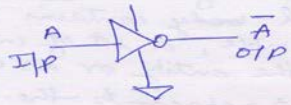
Q.5

a. Draw the block diagram of a general two-stage op-amp and explain the working operation of each block.

Answer:

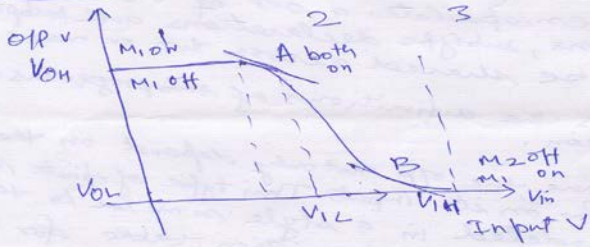
Q5a. The fig below shows the inverter. It performs logic operation

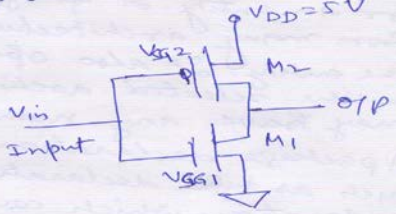




When the input of inverter is connected to ground, the o/p is (in accord with digital models (in the last $A = \bar{A}$)) is pulled to 5V through p-channel transistor. When the I/p terminal is connected to V_{DD}, the o/p is pulled to ground through the n-channel MOSFET.

DC characteristics:



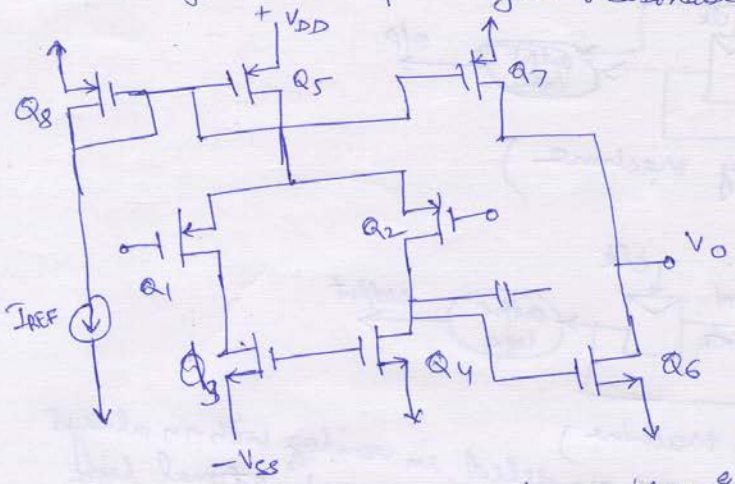


In region 1 of transfer characteristics, the I/p voltage is sufficiently low so that M_1 is off and M_2 is ON. As V_{in} is increased, both M_2 and M_1 turns on. Increasing V_{in} further causes M_2 to turn off and M_1 to turn on fully (Region 3)

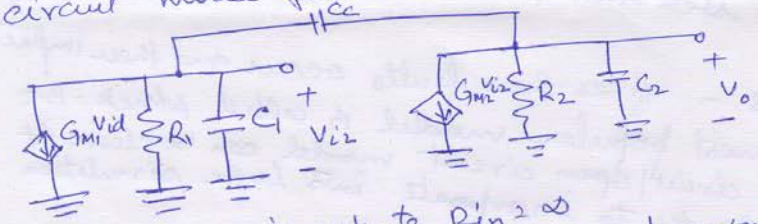
The maximum o/p high voltage is labeled V_{OH} and minimum o/p low voltage V_{OL}. Points A and B on this curve are defined by the slope of the transfer curve. The I/p voltage less than V_{IL} defined by point A are considered as logic low on input of the inverter. Input voltage greater than or equal to V_{IH} defined by point B are considered as logic high on the I/p of inverter. Input voltage between V_{IL} and V_{IH} do not define a valid logic voltage level.

b. Draw the two stage CMOS OPAMP Configuration and calculate its voltage gain.
Answer:

b. the circuit consists of two gain steges. The first stage is (6) formed by differential pair $Q_1 - Q_2$ together with its current mirror load $Q_3 - Q_4$. The differential amplifier circuit provides a voltage gain as well as perform conversion from differential to single ended form while providing a reasonable CMRR.



To determine the voltage gain, consider a simplified equivalent circuit model for small signal operation of cmos amplifier



Input resistance is infinite $R_{in} = \infty$

First stage trans conductance G_{m1} is = trans conductance of each of Q_1 and Q_2 ie $G_{m1} = g_{m1} = g_{m2}$

$$G_{m1} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}} \quad -(1)$$

$$R_1 = r_{O2} \| r_{O4} \quad -(2)$$

$$r_{O2} = \frac{|V_{A2}|}{I/2} \quad -(3)$$

$$r_{O4} = \frac{V_{A4}}{I/2} \quad -(4)$$

$$A_1 = -G_{m1} R_1$$

$$= -g_{m1}(r_{O2} \| r_{O4})$$

$$= -\frac{2}{V_{OV1}} \left| \left(\frac{1}{V_{A2}} + \frac{1}{V_{A4}} \right) \right. \quad -(5)$$

$$G_{m2} = g_{m6} = \frac{2 I_{D6}}{V_{OV6}} \quad -(6)$$

$$R_2 = r_{O6} \| r_{O7}$$

$$r_{O6} = \frac{V_{A6}}{I_{D6}}$$

$$r_{O7} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}} \quad -(7)$$

$$A_2 = -G_{m2} R_2 = -\frac{2}{V_{OV6}} \left| \left(\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|} \right) \right. \quad -(8)$$

Voltage gain

$$A_v = A_1 A_2 = G_{m1} R_1 G_{m2} R_2$$

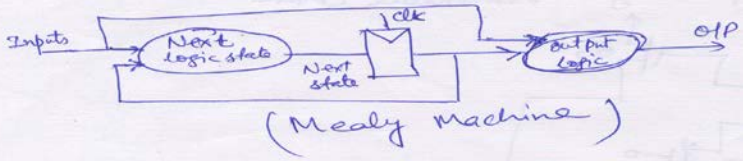
$$= g_{m1}(r_{O2} \| r_{O4})\, g_{m6}(r_{O6} \| r_{O7}) \quad -(9)$$

Q.6

a. Explain finite state machines.

Answer:

Q.6a Finite State Machine: There are two styles of finite state machines. In Mealy machines, the O/P is a function of the current state and inputs. In the Moore machine, the O/P is a function of only the current state.



(Mealy Machine)

(Moore Machine)

Finite state machines are modeled in verilog with an always block defining the state registers and combinational logic defining the next state and O/P logic.

b. Explain fault model in VLSI design.

Answer:

definiting the next

b. Fault Models:- gives how faults occur and their impact on circuits. The most popular model is called stuck-At model. The short circuit/open circuit model can be closer fit to reality, but is harder to incorporate into logic simulation tools.

(i) Stuck at Faults Model: In this model, a fault gate input is modeled at stuck at zero or stuck at one. This model dates from board-level designs where it was determined to be adequate for modeling faults. These faults most frequently occur due to gate oxide shorts or metal to metal shorts. Fig① below

(ii) Short circuit/Open circuit faults includes stuck-open or shorted models. The short results in an S-A-0 fault at point A, while short2 modifies the function of gate. It is evident that to ensure the most accurate modeling, fault should be modeled at transistor level because it is only at high level that the complete ckt structure is known. Figs below

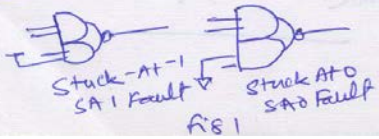


fig 1

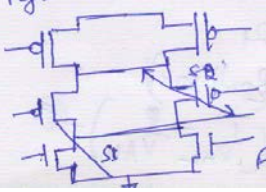


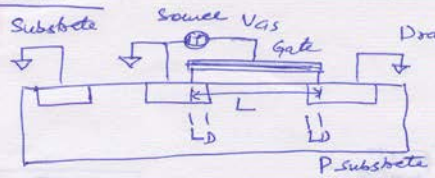
Fig 2

Q.7

a. Explain the importance of scaling of MOS transistor dimensions. Explain the types of scaling and show the effects of parameters in constant voltage scaling.

Answer:

Q.7 a. MOSFET capacitance: Consider the crossectional view of MOSFET. (7) A17/3



The capacitance between gate electrode and substrate electrode is

$$C_{gb} = \frac{\varepsilon_{ox}(L-2L_D)W}{T_{ox}}$$

Where ε_{ox} → dielectric constant

$L-2L_D$ → effective channel length

W → width

The capacitance between gate and the source/drain is simply the overlap capacitance. As we increase Vgs, a capacitance between gate and induced channel under oxide layer exist this capacitor is known a depletion capacitance.

When Vgs is sufficiently large so that a large no. of electrons are attracted under gate, the surface is said to be inverted ie no longer p type. Thus the capacitance from gate to ground changes as Vgs changes for MOSFET configuration. The following capacitance exists in MOSFET

C_{gb} → capacitance associated with gate poly over field region

C_{gd} → drain capacitance

C_{gs} → gate source capacitance

5. (i) Scaling of MOS Transistor dimensions

CMOS technology evolution in the past twenty years has followed the path of device scaling for achieving density, speed and power improvement. MOSFET scaling was propelled by rapid advancement of lithographic techniques for delineating fine lines of 1 μm widths and below. Reducing the source to drain spacing ie channel length of MOSFET led to short channel effects another necessary technology advancement for device scaling is in ion implantation, which is not only allows the formation of very shallow source and drain region but also capacitance of accurately introducing a sharply profiled, low concentration of doping atoms for optimum channel profile design. Scaling can be

- Constant field scaling.
- Generalized scaling.
- constant voltage scaling